UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,406	12/26/2001	Kevin X. Zhang	P11680	8560

7590 09/02/2004

John P. Ward
BLAKELY, SOKOLOFF, TAYLOR &ZAFMAN
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,406	ZHANG ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/15/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 18 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 2, 4 – 5, 7 – 18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamamotto et al. [hereinafter as Yamamotto], US Patent 5,778,237 [cited by applicant in IDS filed on January 15, 2004].

4. As to claim 1, Yamamotto discloses a processor [1, single chip microcomputer] comprising:

a. a voltage regulator [110, power circuit with control circuit 130] to be powered by a first voltage [input voltage at 111 power pin] and to provide a second voltage [113, internal voltage]; and

b. a circuit [101, MULT] powered by the second voltage [113] [col. 2, lines 43 – 64, col. 2, lines 39 – 48, col. 8, lines 55-67, col. 9, lines 1-16].

5. As to claim 11, Yamamotto discloses a computer system [1, single chip microcomputer] comprising:

a. a discrete voltage regulator [110, power circuit with control circuit 130] to provide a global Vcc [input voltage at 111 power pin]; and

b. a processor [100, CPU] including a local voltage regulator [110, power circuit with control circuit 130] to be powered by the global Vcc [input voltage at 111

power pin] and to provide a local Vcc [113, internal voltage] for the processor [100] [col. 2, lines 43 – 64, col. 2, lines 39 – 48, col. 8, lines 55-67, col. 9, lines 1-16].

6. As to claim 18, Yamamotto discloses a computer system [1, single chip microcomputer] and method comprising:

a. providing a first voltage [input voltage at power pin 111] to a processor [1, single chip microcomputer] comprising an integrated voltage regulator [110, power circuit with control circuit 130];

b. powering the voltage regulator [110, power circuit with control circuit 130] with the first voltage [input voltage at power pin 111], the voltage regulator [110, power circuit] to provide a second voltage; and

c. powering at least a portion [powering circuits 101-105 by supplying internal voltage] of the processor [1] with the second voltage [113, internal voltage] [col. 2, lines 43 – 64, col. 2, lines 39 – 48, col. 8, lines 55-67, col. 9, lines 1-16].

7. As to claims 2, 12, and 17, Yamamoto teaches a single chip microcomputer [1, fig. 1] system and method of adjusting [changing] the second voltage [113, internal voltage] with control circuit [130] and voltage setting register [114] [fig. 1] by processor [100, CPU][col. 9, lines 48 – 61].

8. As to claim 4, Yamamoto teaches single-chip microcomputer [1, fig. 1] and method of controlling [changing] clock frequency and operating voltage [internal voltage] with control circuit [130] with changing [switching] frequency of internal clock with first control circuit [131] therefore he teaches timing requirement too [col. 10, lines 48-67, col. 11, lines 1-33][fig. 1].

9. As to claim 5, Yamamoto teaches a port [111,112] to receive the first voltage

[input voltage at power pin 111] from an external voltage regulator [it is inherent to computer system to have a external voltage regulator to convert AC power supply] [fig. 1].

10. As to claims 7 – 10, Yamamoto discloses a digital circuit [a single chip microcomputer 1] includes at least portion of a core of a processor [100, CPU], and a cache memory region [114 voltage setting register, 124 frequency setting register] with direct memory access controller [103, DMAC][fig. 1].

11. As to claim 14, Yamamoto discloses a single chip microcomputer 1 includes at least portion of a core of a processor [100, CPU], and a cache memory region [114 voltage setting register, 124 frequency setting register] with direct memory access controller [103, DMAC] and is powered by the local Vcc [113, internal voltage][fig. 1].

12. As to claim 15, Yamamoto discloses a single chip microcomputer system with CPU [100], which inherently teaches graphic controller.

13. As to claim 18, Yamamoto discloses a single chip microcomputer [1] includes powering a floating point unit [101 MULT, 102 DIVU] of processor [1][fig. 1].

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 3, 6, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamotto et al. [hereinafter as Yamamotto], US Patent 5,778,237 [cited by applicant in IDS filed on January 15, 2004] as applied to claims 1, and 11 above, and further in view of McLoughlin, US 5,932,987.

16. As to claims 3, and 13, Yamamoto teaches a single chip microcomputer [1, fig. 1] and method of changing clock frequency and an operating voltage comprising a voltage regulator [110, power circuit] to be powered by a first voltage [input voltage at 111 power pin] and to provide a second voltage [113, internal voltage]; and a circuit [101, MULT] powered by the second voltage [113] [col. 2, lines 43 – 64, col. 2, lines 39 – 48, col. 8, lines 55-67, col. 9, lines 1-16].

However Yamamoto's voltage regulator [110, power circuit with control circuit 130] does not include a digitized resistor, which is to be set by the processor.

McLoughlin teaches integrated circuit [52, fig. 2] comprises a digitized resistor [52, a digital resistor] set by the processor [with input lines [60] controlled by the microprocessor] and enables microprocessor to control the reference voltage supplied to the DACs [30], which in turn controls the peak output voltage levels of DACs, and to obtain controlled step size with controlled time and smooth transition from zero to operating voltage [col. 5, lines 47 – 49, col. 6, lines 25 – 37] and implemented in integrated circuit [col. 4, lines 56 – 65]. [col. 4, lines 46 – 55].

It would have been an obvious to one of ordinary skill in art, having the teachings of Yamamoto and McLoughlin before him at the time the invention was made, to modify the Yamamoto's power circuit [110] and control circuit [130] to include a digitized

resistor [digital resistor 52] controlled by microprocessor [col. 4, lines 46 – 55, fig. 2] as taught by McLaughlin, in order to control the peak output voltage level and to obtain controlled step size with controlled time and smooth transition from zero to operating voltage [col. 5, lines 47 – 49, col. 6, lines 25 – 37] and implemented in integrated circuit [col. 4, lines 51 – 65].

17. As to claim 6, McLoughlin discloses an op amp [54] [col. 4, lines 46 – 49][fig. 2].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994 [571-272-3675 after October 15, 2004]. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 703-308-1159 [571-272-3670 after October 15, 2004]. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
August 17, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100